

critical gate region wherein the lateral diffusion of the source dopants is decreased and having low V_{ss} resistance, and wherein the EEPROM includes a multitude of field effect transistor memory cells each having a source, drain, a floating gate, a control gate and a substrate, the method comprising:

- (a) forming multiple gates on a substrate defining drain regions and source regions associated with each of the multiple gates;
- b) forming a first source mask exposing the source regions and portions of the gates;
- c) implanting the exposed source regions with n dopant ions;
- d) removing the first source mask;
- e) forming a second mask exposing a portion of the source regions;
- f) implanting the exposed portions of the source region with n^+ dopant ions; and
- g) removing the second source mask;

wherein the edge of the first source mask does not coincide with a (SGE) stacked gate edge adjacent the shared source regions.

5. (Amended) A method of manufacturing a flash memory Electrically-Erasable Programmable Read Only Memory (EEPROM) device having a lightly-doped source region near the critical gate region and a heavily-doped source region away from the critical gate region wherein the lateral diffusion of the source dopants is decreased and having low V_{ss} resistance, and wherein the EEPROM includes a multitude of

field effect transistor memory cells each having a source, drain, a floating gate, a control gate and a substrate, the method comprising:

a) forming multiple gates on a substrate defining drain regions and source regions associated with each of the multiple gates;

b) forming a source mask exposing the source regions;

c) implanting the exposed source regions with n+ dopant ions; and

d) removing the source mask;

wherein the edge of the first source mask does not coincide with a (SGE) stacked gate edge adjacent the shared source regions.